Quarterly report
Chronic Microelectrode Recording Array
NIH/NINDS
Period 03/01/05 – 06/30/05

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I. Executive summary

The overall goal of the contract No. NIH/NINDS HHSN265200423621C is to develop and test (in-vivo) a chronically implantable neural recording array and provide the device to the neuroscience community upon completion of the initial technical development phase for experimental use and evaluation.

The objective of the third quarter (Q3) as proposed was to:

a) Begin work on biocompatible coating modifications and continue fabricating UEA test chips
b) Final design for re-routing layer on UEA
c) Successfully bench test the 1st version signal processor chip
d) Finalize the coil design, proceed with fabrication and possibly begin testing
e) Demonstration of 1st level flip chip bond test assembly (IC on UEA) and preparation of SMD and coil assembly
f) Continued leakage current, impedence spectroscopy, adhesion and dissolution long term tests of SiC and Parylene encapsulation in buffer solution and subsequent further development of Parylene and SiC coating processes, materials characterization (material composition, electrical and chemical properties)

Throughout the third quarter, all the above mentioned objectives (a-f) were accomplished. All modules of the IC work reliably in the 1st version of the IC already with only minor modifications being required for the 2nd version of the chip in order to further improve the processing speed of a few selected components. We have found a way to devise the coil as two single layer coils which can be switched to operate independently, in series or in parallel to compensate for changes in parasitic capacitance and voltage gain. The slightly modified coil concept has caused a minor delay of about 2 weeks, which will not impact the delivery and testing of the entire system. Once again, the results obtained in this quarter further support the validity of the proposed device design and fabrication approach. We have also intensified the cooperation with Dr. Tresco's histology laboratory in order to initiate a) studies on SiC tissue impact b) identify potential additional biocompatible coatings such as various hydrogels.

Furthermore, the first INIP meeting for researchers working on neuroprosthetics at the University of Utah across all schools took place on April 21st 2005. The collected presentation slides were submitted to NIH/NINDS and are available upon request from the project coordinator. Talks and open information exchange were commenced with Innersea and Cyberkinetics.

II. Activity Summary

Key results for project period (Q III) (work packages)

- Fabrication of UEA test and hot chips: fabrication of UEAs was continued. Work was commenced on optimizing fabrication processes and implementing wafer scale processes as opposed to the currently used 3x3 arrays. Furthermore, the final design for the re-routing layer on the UEA was approved.
- Development and fabrication of electronics and communications module: bench testing of all IC components (amplifiers, A/D converters, RF module, power recovery module, etc.) was performed. All modules are fully operational, with only minor flaws (slightly slower processing time as specified for neural signals) which can easily be corrected in the 2nd version scheduled for Setpember.
- Development and fabrication of LTCC ferrite coil: final approval of design after review by simulation, IC, packaging and encapsulation teams at UofU, Fraunhofer IZM and Fraunhofer IBMT. The coil module consists of two single layer Au-electroplate coils with 60 turns each on a Polyimide film and glued to an LTCC platelet. The fabrication of the coil for the final neural interface has commenced.
- Flip-chip bonding and assembly: successful 1st level flip chip bond between UEA and IC and preparation of 2nd level (SMD and coil) assembly and interconnect.
- Hermetic encapsulation and layer coating: continued fabrication of test structures for coating layer adhesion and electrical characterization (acute and long-term), deposition of silicon carbide and parylene layers on test structures, characterization of layer composition, start of electrical testing of layers in saline/buffer solution; continued long term test (leakage currents, impedence spectroscopy, dissolution, adhesion)

Meetings/presentations during project period (Q III)

- First Integrated Neural Interface Program (INIP) meeting on April 21st 2005.
- Telephone conferences with IBMT and IZM
- Individual weekly project meetings of the project teams at the University of Utah as well as the subcontractors; meeting minutes are created in common format by all partners.

Patents (Q III)

- No additional new invention disclosures, further processing of previously submitted invention disclosures

Organizational accomplishments (Q III)

- Employment and training of new technician (again!)
- Temporary replacement of one graduate student currently hospitalized
- Organization of INIP meeting, Logo development for INIP program

III. Research Results and Discussion

III.a. Probe system fabrication

III.a.1 Task 1 Fabrication of ultra thin Utah Electrode Array

Description/Rationale

Conventional Utah Electrode Arrays were built for a variety of testing purposes. Optimization of the backplate thinning process has begun. No further activities were planned for the second quarter.

Future plans for the next two (2) quarters

In the coming two quarters, the polishing process will be finalized for electrode arrays with thinned backplate, including characterization.

III.a.2 Task 2: Development and fabrication of electronics and communications module

Description/Rationale

The electronics/communication module will be a single CMOS integrated circuit mounted on the back of the microelectrode array. Two or three surface-mount capacitors mounted near the chip to provide capacitance values not achievable on chip are planned. The electronics module will amplify and process neural signals, transmit this data out of the body on an RF carrier, and receive power and command data from the power coil via a transcutaneous magnetic link.

Experimental Results

We have received 40 fabricated copies of our first integrated circuit: Integrated Neural Interface chip version 1.0 (INI1). The chip was submitted to MOSIS for fabrication in March 2005 and received in late May 2005. The chips measure 4.88 mm × 6.03 mm × 240 µm. Twelve of the returned chips were packaged in small, 52-pin ceramic packages to facility bench-top testing in Harrison's lab. The remaining 28 unpackaged bare die will be used for flip-chip bonding tests.

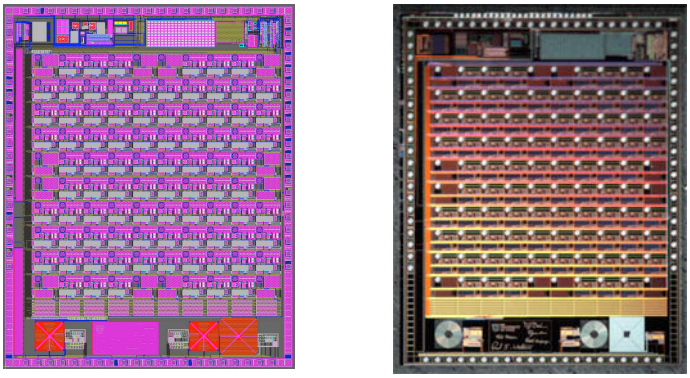

Fig. 1: Layout of Integrated Neural Interface chip version 1.0 (INI1) (left) and photo of fabricated chip (right). The fabricated chip measures 4.88 mm × 6.03 mm × 240 µm and contains over 30,000 transistors and over 5,000 passive components (capacitors, resistors, inductors, and diodes).

- **Power recovery module.** This module interfaces with the power coil and converts the unregulated ac voltage on the coil into a regulated dc voltage to power the chip. We use an on-chip full-wave bridge rectifier to convert ac to dc. A linear voltage regulator with a bandgap voltage reference is used to regulate the power supply voltage at 3.3 VDC. We have successfully built and tested a computer-controlled wireless power/command transmitter that operates at 2.64 MHz.
- **Forward telemetry module.** This module also interfaces with the power coil and performs two functions. First, this circuit generates a stable, digital (square wave) 330-kHz clock synchronized to the oscillation on the coil (divided by eight). This clock serves as a frequency reference for the entire chip. Second, this circuit identifies changes in the amplitude of the ac voltage waveform on the coil. These amplitude changes will be used to send telemetry data (e.g., configuration commands) to the

implanted device. The circuit interprets each amplitude change as a 'one' or 'zero' based on the length of each pulse, and loads this binary data stream into on-chip configuration and command registers. Our current chip has 128 bits of internal configuration bits.

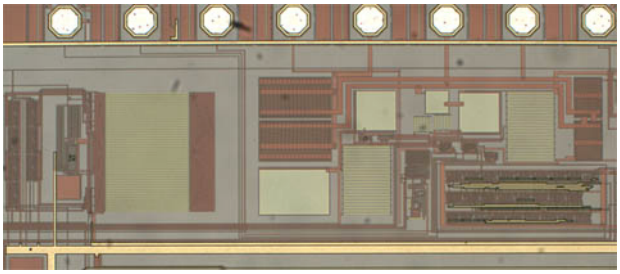

Fig. 2: Photo of INI1 chip showing power recovery and forward telemetry interface circuitry. On-chip diodes rectify the ac power received by the coil, and a digital controller extracts amplitude-modulated data from the power waveform.

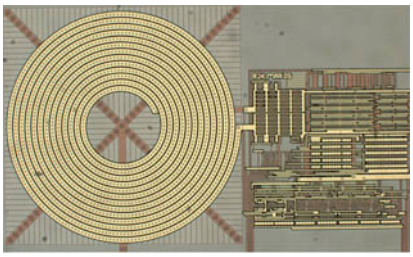

Fig. 3: Photo of INI1 chip layout showing fully-integrated 433-MHz data transmitter. The on-chip planar spiral inductor measures 472 µm in diameter and acts as transmitting antenna.

- **Neural signal amplifiers and spike detectors.** A 10 × 10 array of neural signal amplifiers and spike detector circuits form a 4 mm × 4 mm array at the center of the chip. Each amplifier has an octagonal bond pad 70 _m in diameter that will connect to the microelectrode array. Each amplifier has a gain of 60 dB and a bandwidth from 1 kHz (to block large-amplitude local field potentials) to 5 kHz. A comparator is used to detect spikes by comparing the output of the neural amplifier to a programmable reference level set by an on-chip digital-to-analog converter (DAC).

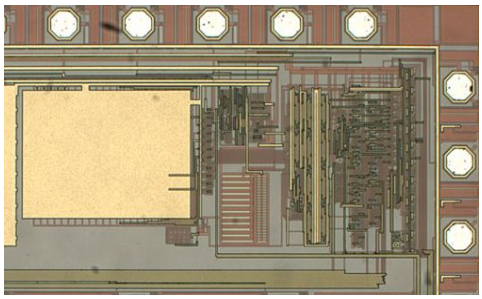

Fig. 4: Photo of INI1 chip layout showing fully-integrated 9-bit analog-to-digital converter (ADC). The circuit utilizes a large capacitor array (left) to implement a low-power charge redistribution architecture.

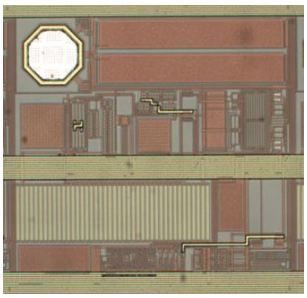

Fig. 5: Photo of INI1 chip layout showing a single neural amplifier cell. The amplifier has a gain of 60 dB and a bandwidth of 1 kHz – 5 kHz. Each cell includes a spike detector for data reduction. The 70-_m octagonal bondpad in the upper left corner contact the UEA.

- **Analog-to-Digital Converter.** The chip has a 9-bit analog-to-digital converter (ADC) to digitize a selected neural waveform at 15 kSamples/s. An analog multiplexer (MUX) is used to route the selected neural amplifier signal to the ADC.
- **RF transmitter for reverse telemetry.** An on-chip RF transmitter transmits the digital data from the ADC and the spike detectors. The transmitter operates in the 433 MHz SRD band at a rate of 330 kbit/s using binary frequency-shift keying (FSK). An optimized on-chip planar spiral inductor minimizes power consumption.

Discussion/Interpretation of Results

We are currently in the middle of benchtop tests of the INI1 chip. Initial tests show basic functionality in all modules. Our voltage regulator successfully converts an ac voltage on a small off-chip coil into a regulated 3.3 VDC on-chip supply. The regulator requires a minimum peak coil voltage of 5.6 V for proper power supply generation. We are currently powering the chip via a 2.64-MHz wireless link in our

laboratory. Command data may be sent to the chip by amplitude-modulating the power waveform. We have sent data at a rate of 6.5 kbit/sec, although we have discovered a bug in our data receiver that leads to prohibitively high bit error rates. The source of this bug is now well understood, and this circuit will be corrected in the next version of the chip to be sent out in early September.

The neural signal amplifiers exhibit a proper gain of 60.1 dB, and a bandwidth ranging from 1 kHz to 5 kHz to isolate spikes. The input-referred noise of the amplifiers is 5.1 V_{rms}. We consider this noise level acceptable, but we aim to improve this parameter in the next design. Spike detectors function as designed, with a programmable detection threshold. The on-chip ADC works to 9-bit accuracy at a sample rate of 15 kS/s. The linearity of this circuit is excellent, with INL and DNL errors of less than ±0.8 LSB. The 433-MHz FSK data transmitter is functional, and we have demonstrated a received signal strength of -85 dBm using a half-wave resonant dipole antenna at a distance of 15 cm while using only the on-chip 54-nH inductor as the transmitting antenna. Preliminary power consumption measurements indicate that the entire chip should consume less than 20 mW of power.

Future Plans for Next Two (2) Quarters

We will continue detailed testing of the INI1 chip and begin design of the improved "version 2" INI2 chip. This chip will be submitted for fabrication on 6 September 2005, and will return from fabrication in mid-November. We are also beginning design of the RF data receiver hardware and software, and a GUI software interface to control the wireless power controller and send commands to the chip.

Description/Rationale

The electronics/communication module is a single CMOS integrated circuit mounted on the back of the microelectrode array. Three surface-mount capacitors mounted near the chip provide capacitance values not achievable on chip. The electronics module will amplify and process neural signals, transmit this data out of the body on an RF carrier, and receive power and command data from the power coil via a transcutaneous magnetic link.

III.a.3 Task 3: Development and fabrication of LTCC ferrite coil

Coil simulations – final design

In order to allow a higher coil density and higher subsequent voltage gain, Polyimide based electroplated Au coils placed on an LTCC platelet are used. The electrical properties of geometrical variations of selected coil designs were simulated. All simulations were done using circular coils, based on numerical calculations using an FEM (finite element method) solver FlexPDE (Antioch, CA, USA) as described in the previous report on LTCC-coil simulations. The minimum spatial resolution with this technology is 4 µm line width and spacing. For higher yield and accuracy, however less challenging dimensions are recommended. The design guidelines for the coil are outlined as: fixed outer dimension: D_{out}=5 mm, line thickness should be as large as possible within technical limitations: h_{max}=20 µm to avoid a very high series resistance of coils caused by a narrow line width, min. line width: w_{min}=10 µm, min. line spacing: s_{min}=10 µm, Cu or Au coils are assumed for the simulation of coil characteristics: conductivity σ=4.64x10^7 S/m (80 % of bulk Cu), operating frequency=2.64 MHz, Diameter of a ferrite substrate=5.5 mm, thickness=200 µm, permeability μ_r=200. The two designs depicted below was investigated with regard to their electrical characteristics and performance in power transmission.

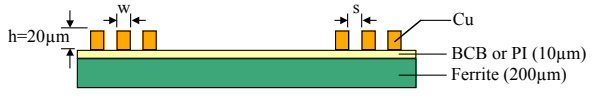

Fig. 6 a: Type I: single layer thin-film coil, attached on a ferrite layer

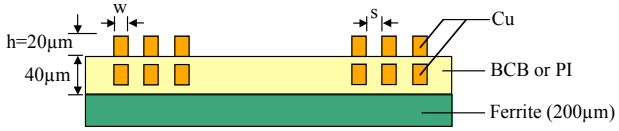

Fig. 6 b: Type II: double-layer thin-film coil, attached on a ferrite layer

Simulation results

Fig. 6A shows the inductance and Q-factor of thin-film coils when the line width/spacing is fixed and the number of turns is increased, decreasing the opened area inside the coil. As already stated in the previous report on coil simulations, Q would be maximum when the windings fill the coil diameter by a factor of about 80 % toward the centre. On the other hand, the inductance increases as the number of windings increases. Roughly, two-layered coils increase the inductance by a factor of 4 and the quality factor by 2, compared to those of single-layer coils. When N=80, type I coil has Q=7, L=40 µH, and the corresponding is C=91 pF; type II coil has Q=14, L=160 µH, and C=23 pF.

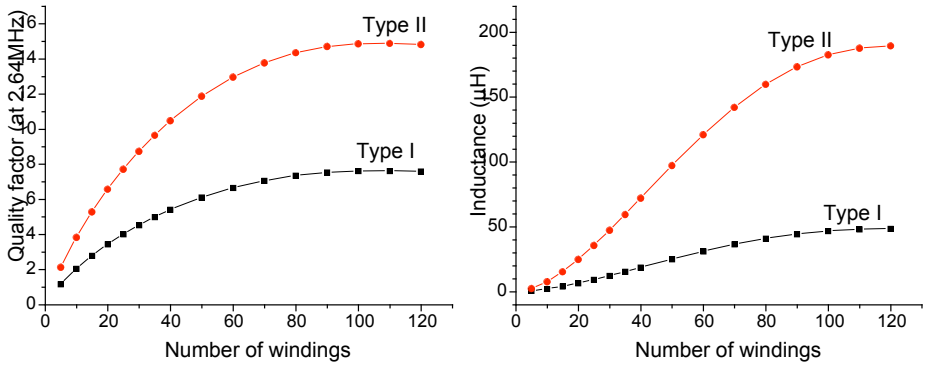

Fig. 7: Quality factor and inductance of two different coil types. The line width and spacing were 10 µm, the height was h=20 µm. A large number of windings mean that the coil fills the diameter more toward the centre.

The impact of line width variations was investigated using a fixed inner diameter of the coil: D_{in}=1.25 mm (i.e. the windings fill 75 % of the coil). Fig. 8 shows the inductance and Q-factor as function of line width and number of turns at constant line spacing s=10 µm. For N=94, the line width is 10 µm, which was considered the minimum width to be technologically feasible. With increasing number of turns (decreasing line width), the inductance increases and the Q-factor decreases. For a line width of 10 µm to 20 µm, an inductance of 20 to 45 µH and Q of 10 to 7.5 may be obtained for the type I coil (single-layer coil); and an L of 77 to 177 µH and Q of 20 to 15 may be obtained for the type II coil (double-layer coil). It can be concluded that single-layer coils may be sufficient for the purpose.

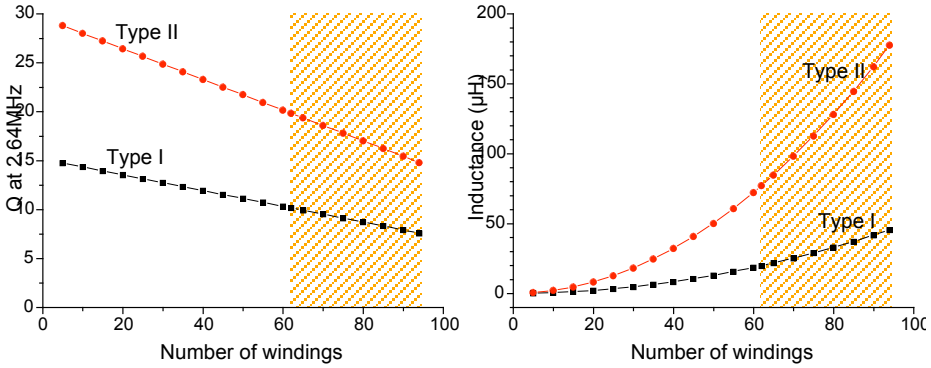

Fig. 8: Quality factor and inductance of two different coil types. For both coils, windings fill the diameter by 75 % from outside to the centre. Line width varies according to the number of windings. A larger number of windings mean that the coil line is narrower. The line spacing and the coil height are fixed as s=10 µm and h=20 µm, respectively.

The influence of the variation in coil height on the coil performance was simulated for: (1) D_{out}=5 mm, D_{in}=1.25 mm, s=10 µm, w=10 µm, N=94 and (2) D_{out}=5 mm, D_{in}=1.25 mm, s=10 µm, w=20 µm, N=62.

The simulation results are shown in Fig. 9. The change in coil height from 10 to 20 µm does not affect the inductance significantly. The Q-factor is increased proportionally with the coil height.

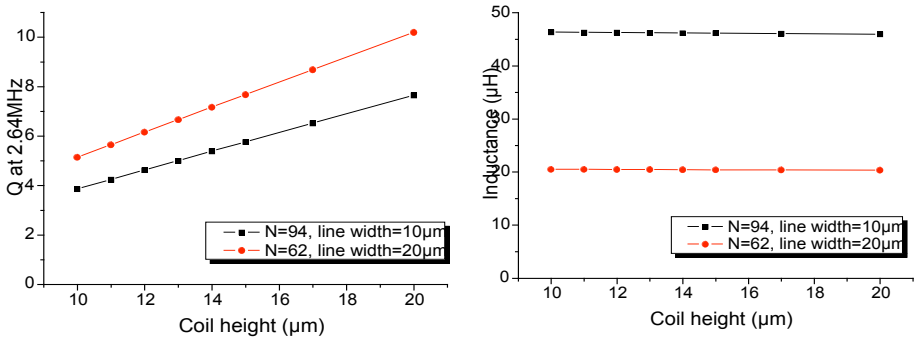

Fig. 9: Quality factor and inductance of two different coil types. For both coils, windings fill the diameter by 75 % from outside to the centre and the line spacing is s=10 µm.

(2b) Thickness of the polymer layer between coil and ferrite substrate

The influence of the distance (d) between coil layer and ferrite substrate on the coil performance was simulated. The inductance increase due to the ferrite substrate is shown in Fig. 10 as a function of the distance between coil and ferrite and comparing it to the inductance when no ferrite was used. With μ_r=200, the inductance increase is 80 % for a distance d=10 µm, and 64 % for d=100 µm.

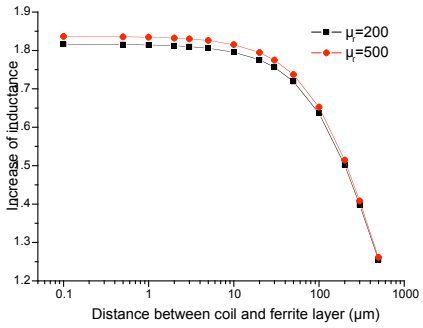

Fig. 10: Influence of the distance between coil layer and ferrite substrate on the coil inductance. The coil configuration used was a single-layer coil having D_{out}=5 mm, D_{in}=1.25 mm, h=20 µm, w=20 µm, s=10 µm, and N=62, resulting in L=20 µH and Q=10.

(2c) Parasitic capacitance of coils

The capacitance between coil windings was predicted by simulation of electric fields (Fig. 11). The inter-winding capacitance of such thin-film coils should be less than 1 pF. A single-layer coil (h=20 µm, w=20 µm, s=10 µm, N=62) has an inductance of 20 µH and a capacitance of 0.15 pF, resulting in a self-resonance at around 90 MHz. If a conductive substrate is located underneath the coil, (e.g. a silicon IC), a parasitic capacitance between coil and substrate is created. This capacitance is typically much larger than the capacitance between windings (Fig. 11 left/right). If a conducting layer is located sufficiently apart from the receiving coil, (e.g. by the thickness of a ferrite platelet placed between them), the parasitic capacitance between coil and IC may be about 30 pF. Considering the coil-to-substrate capacitance together with the inter-winding capacitance, the total parasitic capacitance of the coil would be 7.65 pF. This would result in a self-resonance frequency of around 13 MHz.

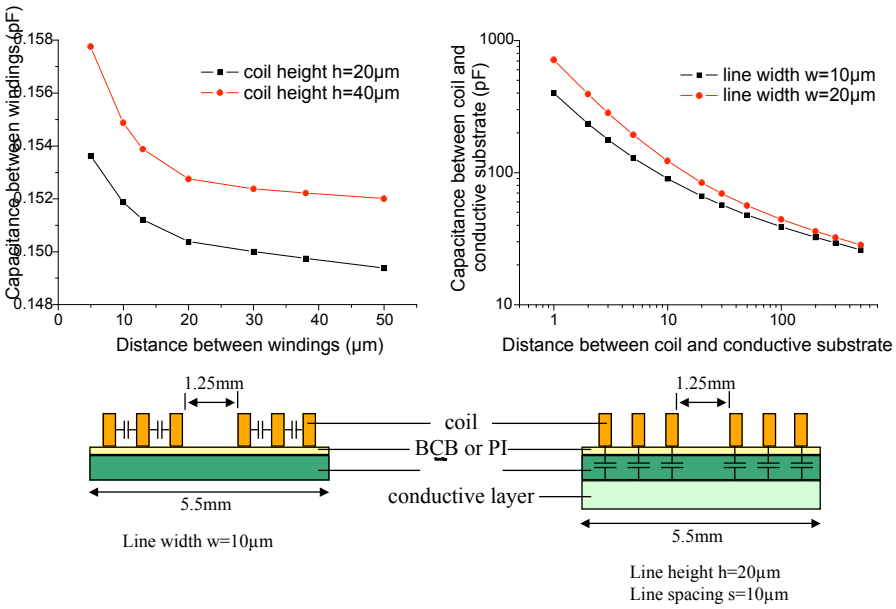

Fig. 11: Capacitance between coil windings (left) and the capacitance between coil layer and a conductive substrate (right).

(2d) Power transmission

A transmitting coil built at the University of Utah was used for the power transmission (diameter 2.2 cm, 17 turns, 0.66 mm diameter wire, 1.14 mm diameter including insulation). The measured inductance of this coil was 6.03 µH and a series resistance was 0.074 ohm. The coupling between the transmitting and receiving coils was predicted as to be about 0.012 through simulations. For higher biocompatibility simulation of coils using Au metallization were performed. The electrical properties and power transmission performance of two types of coils are listed in Table 1. To see the coil performance, the bandwidth and voltage gain (the ratio of the voltage obtained at the load to the voltage over the transmitting coil) were calculated.

Table 1: Electrical properties and power transmission performance of two coil types. The outer diameter is D_{out}=5 mm, the inner diameter D_{in}=1.25 mm, and the coil thickness h=10 µm. The line width and spacing have the same value of 20 µm, 15 µm and 10 µm and the corresponding number of windings is N=47, 63, and 94.

	Type I (single-layer thin-film Au coil on ferrite)			Type II (double-layer thin-film Au coil on ferrite)		
	w=s=20µm	15µm	10µm	20µm	15µm	10µm
Inductance (µH)	12	20	46	45	80	180
Series resistance (ohm)	63	112	251	126	224	502
Q at 2.64 MHz	3.0	3.0	3.0	5.9	5.9	5.9
Parasitic capacitance (pF)	0.13	0.12	0.12	13.2	13.9	14.6
Self-resonance (MHz)	127	103	68	6.5	4.8	3.1
Bandwidth (MHz)	0.43	0.43	0.43	0.32	0.33	0.34
Voltage gain, w/o tuning cap.	0.017	0.022	0.034	0.033	0.043	0.066
Voltage gain, with tuning cap.	0.051	0.066	0.099	0.18	0.24	0.33

Table 2 summarizes the influence of the variation in coil height on the coil performance. The increase in coil height increases the Q-factor of the coil and as a consequence, increases the voltage gain. A coil with

20 µm height would provide twice the voltage gain that could be obtained with a coil having 10 µm height, if a tuning capacitance is used.

Table 2: Electrical properties and power transmission performance of a coil according to the height variation. The used coil configuration was a single-layer coil with D_{out}=5 mm, D_{in}=1.25 mm, w=15µm, s=15 µm, and N=60.

	Coil height		
	h=10 µm	h=15 µm	h=20 µm
L (µH)	19.9	19.8	19.8
R (ohm)	110	73	55
Q at 2.64 MHz	3.0	4.5	6.0
Parasitic capacitance (pF)	0.13	0.13	0.13
Self-resonance (MHz)	99	99	99
Voltage gain without C	0.023	0.023	0.023
Voltage gain with C	0.066	0097	0.13

(2) Coil Design

The electrical properties and power transmission performance of several conceivable thin-film coil designs were simulated and predicted. For all coil designs, a ferrite substrate will be attached under the thin-film coil to increase the self-inductance of the coils. When the distance between the coil and the ferrite substrate (equal to the thickness of BCB or polyimide and adhesive) is 10 to 30 µm, the increase in inductance may be 80 to 75 %. It is recommended that the windings fill the coil diameter by 80 % because this enables the quality factor of the coil to be maximized. With line widths and spacings of 10 µm to 20 µm, 94 to 47 windings can be realized. Increasing the coil thickness improves the power transmission. The minimum required voltage gain between the transmitting and receiving coils is 0.1. Single-layer thin-film Au coils with a line width and spacing of 10 µm to 20 µm may not deliver enough power to the receiving coil even when a ferrite substrate is used. Double-layer thin-film Au coils can provide a sufficient voltage gain. For double-layer coils however, the parasitic capacitance of the coil and the corresponding self-resonance frequency has to be taken into account. For example, a double-layer Au coil with 15 µm line width and spacing would result in a self- resonance at 4.8 MHz, which is still above the operating frequency but quite near to it. The bandwidth of the thin-film Au coils will be around 300 to 400 kHz when the operating resonance frequency is 2.64 MHz. This bandwidth should be sufficient for the purpose. A coil design as shown in Fig. 12 may cause problems in coating the coil surface, due to a high aspect ratio of the structure. It was suggested to encapsulate the coil completely by BCB or polyimide during the process, as shown below. Through the field simulations, it was shown that the inter-winding capacitance of such encapsulated coils may roughly be twice the capacitance of non-encapsulated coils as shown in Fig. 12 .

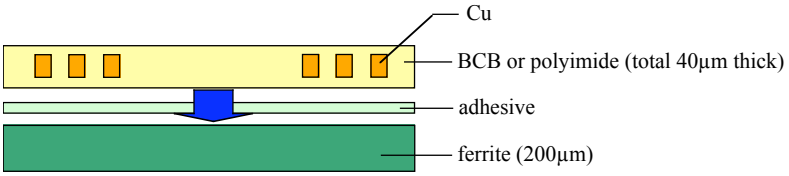

Fig. 12: Assembly of polyimide encapsulated coil on LTCC ferrite platelet.

Coil fabrication – final design

Description/Rationale

Taking into account final technological considerations the coil design, UEA-re-routing and the device assembly were the coil mask design was decided.

Experimental Results

Coil design: Single and double layer coils will be manufactured with 15 µm line width and spacing and a thickness of 10 µm of the Au layer. 60 turns can be realized on each layer. When using double layer coils, the interwinding capacitance could influences the resonance frequency of the coil. A solution is the use of stackable coils. An appropriate layout for the interconnects of the coils for was designed. The schematic in Fig. 13 depicts the routing layout and dimensions of the package. Three different variations can be assembled with this method: 1) a double layer coil, 2) a single layer coil and 3) two stacked coils (a double and a single or two single coils).

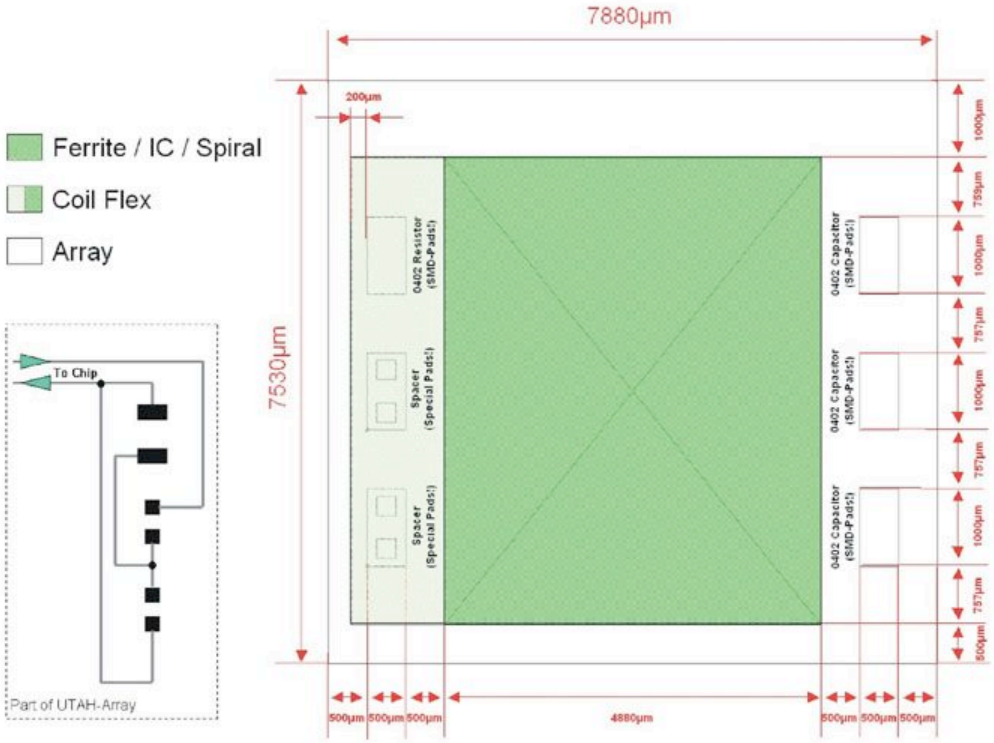

Fig. 13: schematic of the dimensions of the package; the two spacers and the jumper on the left side can be used for single or double coil assembly, the circuit plan is shown on the bottom left side

Discussion/Interpretation of Results

A flexible coil concept was developed to compensate for changes in parasitic capacitance, resonance frequency and voltage gain.

Future Plans for Next Two (2) Quarters

The final (production) coils will be manufactured and tested and the ferrite mounting process will be developed.

III.a.4 Task 4: Flip-chip bonding and assembly

Description/Rationale

Experiments for Au/Sn reflow soldering with a prototype of a handling tool made out of brass were performed. In addition the design of the spacer which will be used for the interconnection between coil and UEA and the design of the coil itself is fixed. An Au/Sn bumped Si monitor wafer with test ICs having the same size and thickness as the functional ICs was manufactured for using it during the assembly setup phase. Finally the Au/Sn reflow soldering of a test UEA with a test IC was successfully carried out.

Experimental Results

Au/Sn reflow: University of Utah designed and manufactured a brass holder for assembly and shipping of the UEA. To simulate the Au/Sn reflow, Au/Sn solder paste was deposited on top of an UEA which was fixed by the holder. The melting of the solder was observed heating up the reflow oven to 340 °C. The following changes of the holder design were suggested by IZM: a) reducing the thickness of the holder to a minimum to reach a better heat transfer, b) fabrication of holders for single modules. Test chips were manufactured using a Si monitor wafer with 240 µm thickness. After Au/Sn electroplating the wafer was diced to get chips with the same dimensions as the functional ICs. The University of Utah provided test UEAs with Au top metallization. A setup was performed with these test UEAs and the test ICs and successful Au/Sn reflow soldering was realized (Fig. 14).

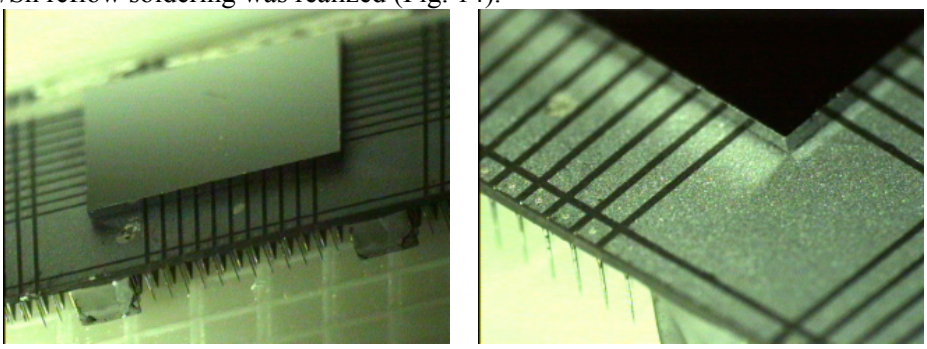

Fig. 14: Au/Sn reflow soldered test IC on a test UEA

Spacer: A ceramic spacer was designed. The spacer will be used for the interconnection between UEA and coil. The size of the component was set to match the size of a 0402 SMD with 1000 µm x 500 µm and a thickness of 508 µm. Fig. 15 shows the schematic of the device.

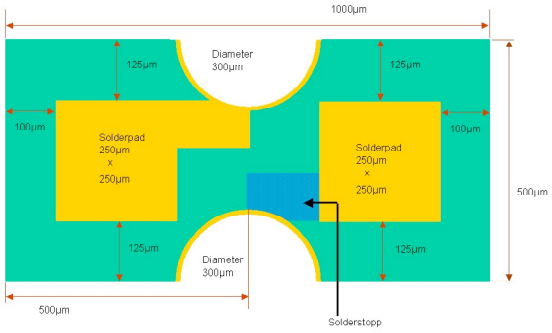

Fig. 15: schematic of the top and bottom side of the spacer

Assembly process: The five step assembly process is shown in Fig. 16.

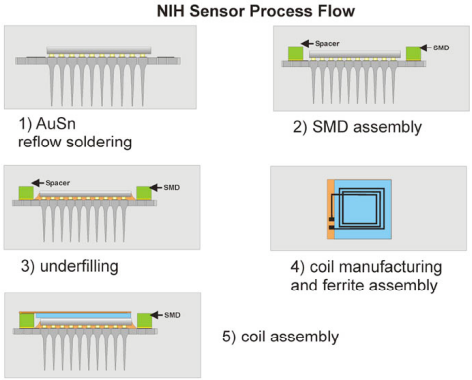

Fig. 16: Assembly process of the sensor package

Discussion/Interpretation of Results

The design phase of the UEA, the spacer and the coil is finished. The first process step, the Au/Sn reflow soldering of the IC on the UEA, was successfully tested.

Future Plans for Next Two (2) Quarters

Test ICs will be Au/Sn reflow soldered on UEA substrates to qualify the assembly process, i.e. the Au/Sn reflow soldering with analysis of the interconnections by cross sectioning, the SMD and coil mounting and the underfilling. Finally, about 10 functional sensor packages/complete neural interfaces will be assembled in Phase I of the project.

III.a.5 Task 5: Hermetic encapsulation and layer coating

III.a.5.1 SiC coating

Films of a-SiC continue to be deposited, and we measure their properties and perform accelerated aging test. The step coverage on the UEA geometry and adhesion of the layers will also be analyzed using SEM and a modified tape peel test.

III.a.5.2 Parylene coating

Description/Rationale

Several investigations were performed to characterize the possible Parylene C encapsulation of the whole device (electrode array with transmission electronic and coil).

(1) Bubble density test: To estimate the quality of thin-film Parylene C encapsulations a bubble test was done. This investigation shows if a layer is pinhole free to ensure the needed encapsulation properties. 300 nm Au layers were sputtered on Pyrex glass wafers. The wafers were diced into 20 mm squares. Cooner wire was hand-soldered to the Au using silver glue with epoxy base (H20E, Polytec). The wires were mechanically fixed to the samples using silicone glue, which also works as a stress release layer for the connection. Parylene C of 1 µm thickness was coated over the samples. The ends of the wires were exposed after the coating was accomplished. The samples were subjected to impedance spectroscopy and the values were compared with results from literature. A destructive bubble density test was carried out with the samples to detect the pinholes and micro cracks in the deposited Parylene C layer.

Experimental Results

(1) Bubble density test:

(1a) Impedance Spectroscopy: The impedance curves were plotted on a solartron 1255 frequency analyzer in combination with a galvanostat 1287. The measurement was carried out in 0.9 % NaCl solution using a three-electrode setup (Fig. 17) with 50 mV amplitude against a silver-silver chloride (Ag/AgCl) reference electrode. A platinum (Pt) electrode was used as counter electrode. The Parylene C coated samples served as the active electrode. Impedance magnitude of Parylene C coating in the range of 100 Hz to 100 kHz was plotted. The values measured at 1 kHz was compared to a back calculation using Parylene C ε_r obtained from the literature.

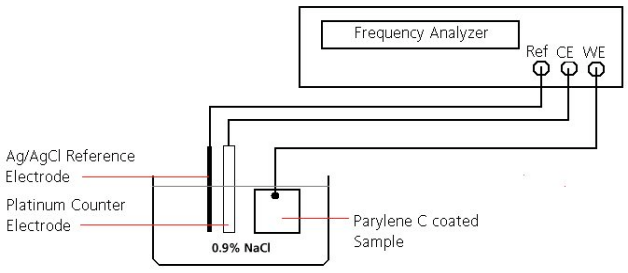

Fig. 17: Schematic, three point electrode setup for impedance measurement of Parylene C coating.

(1b) Investigation on bubble density: the test uses the phenomenon of hydrogen gas evolution from gold surfaces, when immersed into water, on application of voltages more negative with respect to the anode than the redox potential of gold (+1.36 V at 25 °C). The bubbles formed by hydrogen gas evolution Eqn. 1 due to reduction of the gold were an effective method of detection of leakages due to pinholes and micro cracks on the coating by visual examination.

$$2H_2O + 2e^- \rightarrow H_2 + 2OH^- \qquad \text{Eqn. 1}$$

The samples from the impedance measurement with thickness of 1 µm were used in this experiment. The set up was connected to an impedance spectroscope (solartron 1255 frequency analyzer in combination with a galvanostat 1287) in a three-electrode arrangement that consists of an Ag/AgCl reference electrode with a Pt counter electrode. The sample acts as the active electrode. A pulse waveform of –10 V was applied for 10 s across the sample and the counter electrode. The "CorrWare" software was used to control the pulse. The presence of pinholes and micro cracks was detected using the hydrogen bubbles on the surface of the coating and was visually quantified by counting the number of bubbles per unit area.

(1c) Simulation of electrical insulation: the simulation was done in FlexPDE software and problem of computation of field around a plate capacitor was used. The area of the metallization was 10 µm x 10 µm representing a 1 V source. A standard conductivity value from literature was used for the stimulation (resistivities: Au: 56×10^2 1/Ωmm, Parylene C: 0.2×10^{-17} 1/Ωmm, NaCl: 0.03×10^2 1/Ωmm). The Electric field strength E is proportional to the first order differential of the applied voltage. The absolute value of electric field strength *E(abs)*(Eqn. 2) was computed for various corner radii to obtain the maximum of field strength at the corners.

$$E(abs) = \sqrt{(-\partial u/\partial x)^2 + (-\partial u/\partial y)^2} \qquad \text{Eqn. 2}$$

Discussion/Interpretation of results

(1) Bubble density test

(1a) Impedance Spectroscopy: Fig. 18 shows the Impedance spectrum of a 1 µm thick Parylene C layer coated across an area of 371.725×10^{-6} m^2. The capacitive nature of the coating was shown by the approximately –90° phase shift (within limits of machine and measurement error) in the measured frequency range. At 1kHz frequency the Parylene C shows an impedance magnitude of 15.907 kΩ. At this frequency the capacitance of Parylene C was 10^{-8} F. The Parylene C impedance was also calculated using a standard value ε_r=3.1. The measured value also agrees with the calculated values (Table 3).

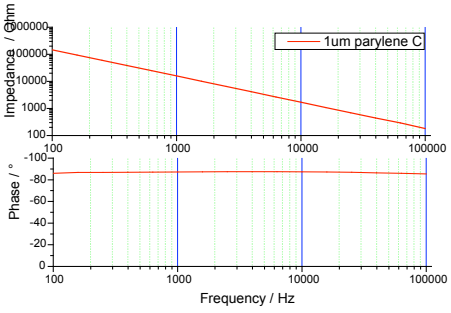

Fig. 18: Impedance magnitude and phase of Parylene C coated samples of the area 371.725 E-6 m^2.

Table 3: Comparison of $|Z_{1kHz}|$ of 1 µm Parylene C layer.

Thickness PPXC / µm	Calculated Values / kOhm	Measured Values / kOhm
1	15.613	15.907

(1b) Bubble test: the bubble test validate the impedance measurements of the Parylene C coated samples because the impedance could be affected by leakage paths due to presence of micro cracks and pinholes in the Parylene C coating. Bubbles on the order of several hundred micrometers diameter were found at

the edge of the samples (Fig. 19). The flat surface coated with Parylene C was devoid of bubbles showing that the coating was pinhole free at 1 µm thickness. The occurrence of the bubbles on the edge may be due to mechanical abrasion of the edges of the samples while coating or due to the inherent stress of the Parylene C layers. The possibility of defects due to breakdown of electrical insulation was simulated.

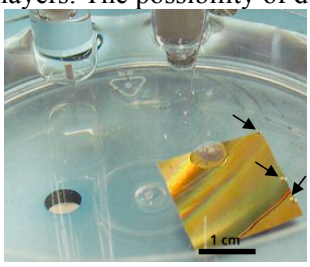

Fig. 19: Bubbles on corners of Parylene C coating on gold sputtered samples of 20 mm X 20 mm size

Fig. 20 shows the results of the simulation for a voltage of 1V. The field strength increases as function of reduced corner radius. A factor 10 increase in the voltage was approximated. The dielectric strength of the Parylene C is 200 MV/m. The applied voltage was 10 V/µm, which is equivalent to 10 MV/m. Including the edge factor, the voltage across Parylene C would be 100 MV/m. This is within the limit of dielectric strength of Parlyene C. Therefore the possibility of an electrical breakdown could be ruled out.

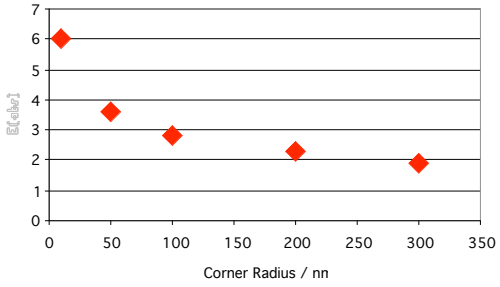

Fig. 20: Electric field strength around corners of different radiuses.

Future plans for the next (2) quarters

Several tests regarding the adhesion of Parylene C on SiC are ongoing. Surface modifications of the SiC layer to improve the adhesion of the Parylene film as well as Parylene peel tests with different treated SiC surfaces are currently under way or planed. For these tests a relatively high amount of samples is required to obtain statistically relevant results. To investigate the thickness uniformity and conformity of the Parylene C layer on the Utah Array electrode tips, the spikes of the array will be partially grinded and polished down. The cross section will be investigated suing SEM. A redesign of the leakage current setup is ongoing and will be finished by the end of August. Besides the fabrication of new analysis modules the system software has to be completely re-designed. The new setup will allow controlling a maximum of 8 leakage current modules with 16 sample holders each.

III.b.1 Task 6: Testing and validation of probe systems (in-vitro/in-vivo)

n/a at this stage of the project except for definition of test program

III.b.1.1 Bench testing of interface/electronics

n/a at this stage of the project

III.b.1.2 In-vivo testing of interface

No in-vivo testing at this stage of project

IV. Concerns

No major deviations or delays have occurred during the third quarter. We would however like to notify NIH/NINDS of one slight deviation from the original plan which from our current perspective does not impact the schedule and outcome of the project:

- The only concerns relate to a continuous slight understaffing of our team due to the delays in finding a suitable technician which could only be found as of June 1st 2005 after the last technician decided at short notice to return to University as a student. Furthermore, one graduate student working on assembly and packaging issues was hospitalized and will remain unable to contribute for at least 1 months time.

Salt Lake City, Utah, June 6th 2005

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